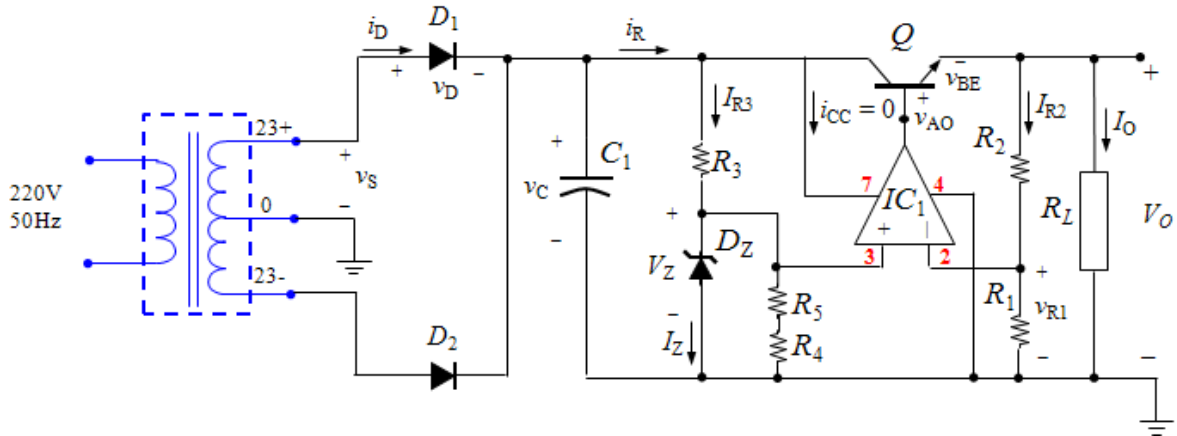


**Subject:** Electronic Systems (SIEK). **Degree(s):** Industrial degrees  
**Professors:** J.A. Soria, X. Roset i R. Ramos  
**Exam Type:** 2nd midterm. **Date:** Wednesday the 11th of June, 2014

### Exercise 1. DC Power Supply



**Figure 1.** Electric diagram of the DC-power supply.

The circuit of Fig. 1 is a DC *Power supply* which consists of a two-phase half-wave rectifier (with central connection to ground) a capacitor-based voltage filter and a voltage regulator, where the OPAMP ( $IC_1$ ) is considered **ideal**, the zener ( $D_Z$ ) operates in the **breakdown** region and the BJT operates in the **active** region. Assuming the component values and semiconductor specifications (indicated below) determine the following information:

#### A) Output voltage $V_O$ :

- a1) Express the output voltage  $V_O$  as a function of the zener voltage ( $V_Z$ ) and the remaining components of the regulator circuit and determine its value.
- a2) What is the minimum voltage required at  $V_{(7)}$  so that the OPAMP operates correctly in the **linear region**?
- a3) What would be the value of  $V_O$  if the non-inverting terminal of the OPAMP (3rd pin) is connected between  $R_4$  and  $R_5$ ?

#### B) Regulator input voltage ( $v_C$ ) and zener ( $D_Z$ ):

- b1) Obtain the maximum voltage drop at the capacitor  $V_{Cmax}$  and specify the current flow through the resistor  $R_3$  ( $I_{R3}$ ) in this condition.
- b2) Demonstrate, by means of determining  $I_Z$ , that the zener is operating in the breakdown region as expected.

#### C) Capacitor $C_1$ and input rectifier diodes ( $D_1$ and $D_2$ ):

- c1) Considering that the user connects an  $I_O = 0.5A$  load, determine the electric current  $I_R$  and specify the necessary capacitor value  $C_1$  to obtain a voltage ripple  $V_r = 5V$  (**Remark:** Assume  $I_{CC} = 0$ ; and that  $I_R \gg I_{R3}$  ( $I_{R3} \approx 0$ ). If you did not manage to obtain  $V_{Cmax}$  at the previous section, use  $V_{Cmax} \approx V_{Smax}$ ).

- c2) Assuming this situation, obtain the following data:  $V_{RRM}$ ,  $I_{D(av)}$ ,  $I_{Dmax}$  i  $I_{D(SURGE)}$ . Taking into account the specifications of  $D_1$  and  $D_2$  provided below, specify whether this semiconductor is suitable for the DC power supply at hand. Provide a reason for your answer.

**Component DATA:**

- Transformer:

*1st winding: 220V/50Hz.*

*2nd winding: +23/0/-23 Volts (root mean square value)*

- Resistors:  $R_1 = 10k\Omega$ ;  $R_2 = 15k\Omega$ ;  $R_3 = 1k8\Omega$ ;  $R_4 = 12k\Omega$ ;  $R_5 = 100k\Omega$
- $D_Z$ : BZX85V10 –  $\{V_Z = 10V$ ;  $I_{ZT} = 1mA$ ;  $P_Z = V_Z I_{Zmax} = 1W\}$ .
- $I_{C1}$ : LM741 –  $\{V_{DROP\_OUT} = 2V$  on  $V_{AOmax} = V_{(7)} - V_{DROP\_OUT}\}$ .
- $Q$ : BD243C –  $\{\beta = 75$ ;  $V_{Be\gamma} = 0.7V$ ;  $V_{CESAT} = 0.5V\}$ .
- $D_1 = D_2$ :  $\{V_\gamma = 0.7V$ ;  $V_{RRM} = 50V$ ;  $I_{DMAX} = 15A$ ;  $I_{D(SURGE)} = 40A\}$

## Exercise 2: Digital Systems

A digital system needs to be designed for controlling the amount of light present in a windowed room (Fig. 1). The system consists of three fluorescent lamps: A, B and C; which have to be turned on (HIGH level logic “1”) when the ambient light is not enough to illuminate the room.

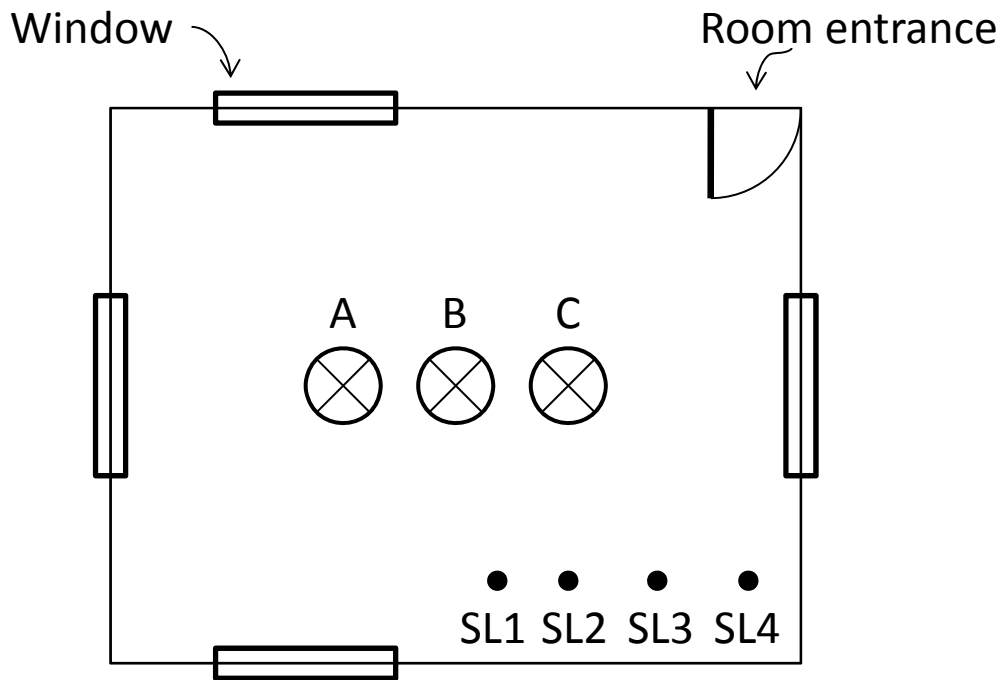


Figure 1. System layout of the room

Four light sensors detect and measure the ambient light outdoors: SL1, SL2, SL3 and SL4; and they operate in the following manner:

- **SL1** is activated (HIGH level logic “1”) when the ambient light is **equal or over 700 LUX**, and deactivated otherwise (LOW level logic “0”).
- **SL2** is activated (HIGH level logic “1”) when the ambient light is **equal or over 750 LUX**, and deactivated otherwise (LOW level logic “0”).
- **SL3** is activated (HIGH level logic “1”) when the ambient light is **equal or over 800 LUX**, and deactivated otherwise (LOW level logic “0”).
- **SL4** is activated (HIGH level logic “1”) when the ambient light is **equal or over 900 LUX**, and deactivated otherwise (LOW level logic “0”).

The illumination system also has a mechanism for sensor fault detection, for instance, when then sensor SL2 is activated and SL1 is not. In all these similar cases, an **ALARM** indicator is activated (HIGH level logic “1”) and **ALL fluorescent lamps must be turned off**.

On the other hand, when the **ALARM** indicator is not activated, the system operates correctly and the fluorescent lamps must be turned on according to the following behavior pattern:

- The **fluorescent lamp A** is turned ON when the outdoor light is **lower** than **900 LUX**, and is turned OFF otherwise.
- The **fluorescent lamp B** is turned ON when the outdoor light is **lower** than **750 LUX**, and is turned OFF otherwise
- The **fluorescent lamp C** is turned ON when the outdoor light is **lower** than **700 LUX**, and is turned OFF otherwise

**Design process:**

**a)** Write the “truth table” corresponding to the logic functions which control the turning ON and OFF of the fluorescent lamps, and the ALARM indicator, according to the outdoor sensors.

**b)** Find the **simplified** logic functions that control the turning ON and OFF of the fluorescent lamps, and the ALARM indicator. Use the Karnaugh-maps method.

**c)** Obtain the full circuit necessary for implementing this system by means of AND, OR and NOT gates (**Remark:** logic gates can be of several input terminals).

**d)** Represent the electric circuit corresponding to the ALARM indicator using only 2-input NAND gates.

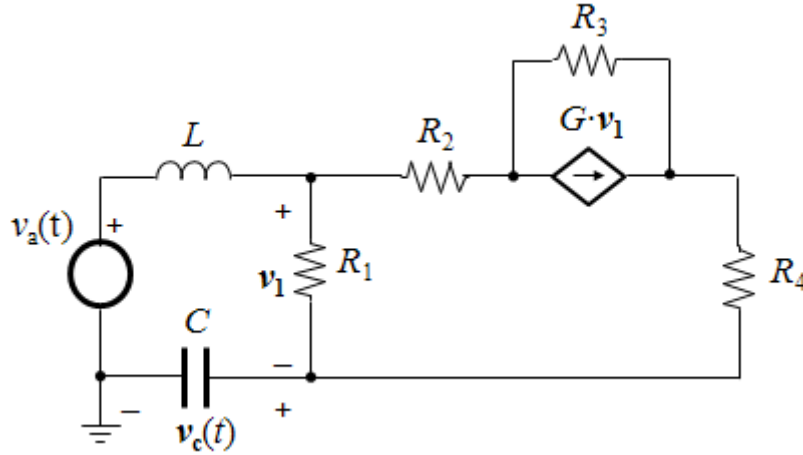
**Subject:** Electronic Systems (SIEK). **Degree(s):** Industrial degrees

**Professors:** J.A. Soria, X. Roset y R. Ramos

**Exam Type:** 1<sup>st</sup>. midterm (retrieval). **Date:** Wednesday the 11<sup>th</sup>, of June, 2014

**Exercise.** Steady-state and time domain (10 points).

In the following circuit, assuming **zero** initial conditions in L and C



**Figure 1.** Electric diagram of the circuit corresponding to Exercise 1.

- a) Determine the normalized 2<sup>nd</sup>-order transfer function of the. Use the basic analytical methods and express the factor gain **K**, the damping factor  $\xi$  and the natural frequency  $\omega_n$  as a function of the circuit components, and indicate the units of the constant **G**

$$H(s) = \frac{v_c(s)}{v_a(s)} = K \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (1)$$

- b) Assuming that the circuit transfer function (2) is associated to the circuit (Fig. 1), represent the output waveform  $v_c(t)$  for a step input,  $v_a(t) = 2 \cdot u(t)$ :

$$H(s) = \frac{v_c(s)}{v_a(s)} = \frac{210000}{s^2 + 190s + 100000} \quad (2)$$

**Remark:** You must determine the relevant points of the output signal: **SIP** (overshoot),  $t_p$  (peak time),  $t_r$  (rise time),  $t_s$  (settling time: signal within a 5% of output variation in  $v_c(t)$ ) and final value of  $v_c(t)$ .

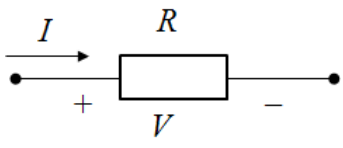
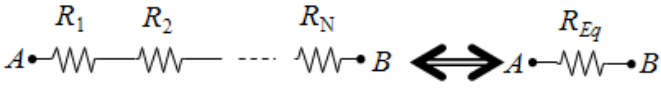
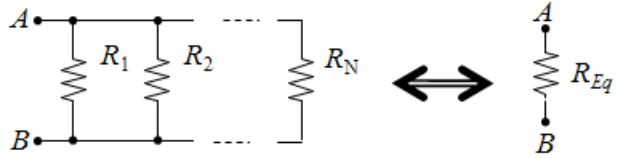
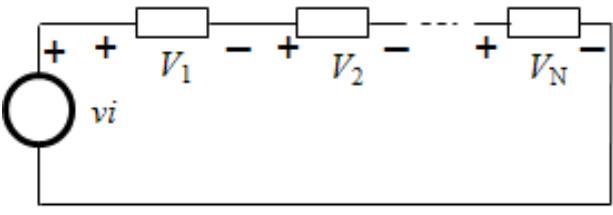
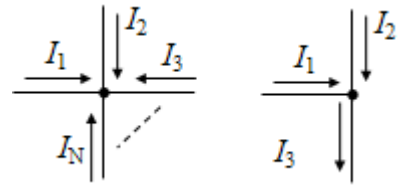
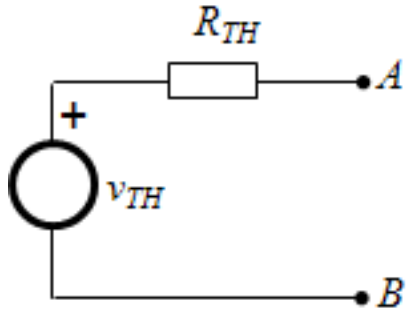
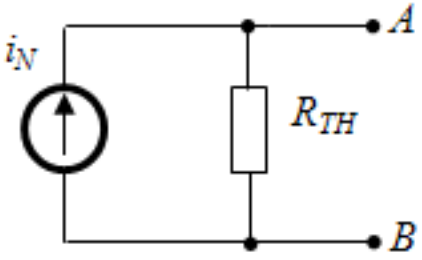
- c) Taking into account the transfer function in (2), determine the output voltage  $v_c(t)$  on a permanent-state basis for a sinusoid input of the form  $v_a(t) = 10 \cdot \sin(2 \cdot \pi \cdot 20 \cdot t)$ , where  $f = 20\text{Hz}$ .

**Remark:** You must specify the output expression  $v_c(t)$ , as a function of the input  $v_a(t)$ , and draw both signal waveforms in the same plot, specifying both the peak magnitude and the time values associated to the phase shift between both signals.

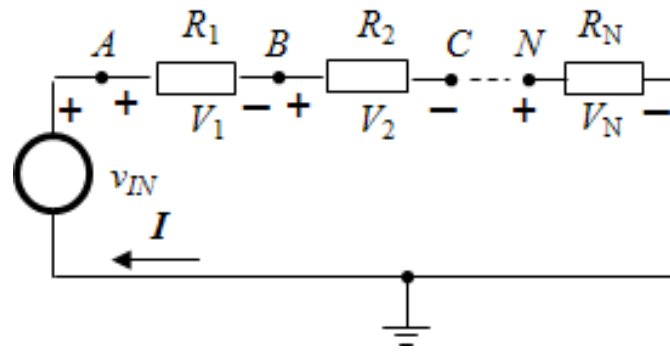


# Expression Form SIEK

## 1 – Basic electrical rules in circuit analysis: steady-state (DC) and time domain operation (AC)

Ohm's law	
	$V = R \times I \quad I = \frac{V}{R} \quad R = \frac{V}{I}$ <p><b>*Sign convention:</b> Electric current entering the positive pole</p>
Resistor connection	
<p><b>Series</b></p>  $R_{EQ} = R_1 + R_2 + \dots + R_N$	<p><b>Parallel</b></p>  $R_{EQ} = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \dots + \frac{1}{R_N}}$ <p><b>*Two resistors:</b> <math>R_{EQ} = \frac{R_1 R_2}{R_1 + R_2}</math></p>
Kirchhoff's Laws	
<p><b>KVL (1<sup>st</sup>. Voltage law)</b></p>  $v_i - V_1 - V_2 - \dots - V_N = 0$ $v_i = V_1 + V_2 + \dots + V_N$ <p><b>* SOURCE = Addition of all voltages in series</b></p>	<p><b>KCL (2<sup>nd</sup>. Electric Current Law)</b></p>  $I_1 + I_2 + \dots + I_N = 0$ $I_3 = I_1 + I_2$ <p><b>* All ENTERING intensities = All OUTGOING currents</b></p>
Thevenin/Norton Changes	
<p><b>Thevenin Model</b></p>  <p><math>R_{TH} = R_N</math></p>	<p><b>Norton Model</b></p>  <p><math>R_N = R_{TH}</math></p>

# Voltage Divider / Difference in voltage potential (For voltages referred to the GROUND terminal)



**Voltage divider**

**Difference in voltage potential**

$$V_i = \frac{R_i}{\sum_{i=1}^N R_i} v_{IN}$$

$$I = \frac{V_A - V_B}{R_1} = \frac{V_B - V_C}{R_2} = \dots = \frac{V_N - 0}{R_N}$$

\*Example obtaining  $V_2$ :

\*  $V_A, V_B, \dots, V_N$  correspond to circuit node voltages referred to ground

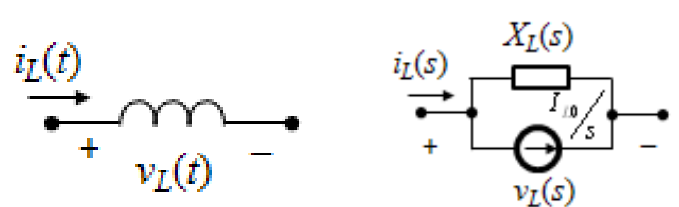
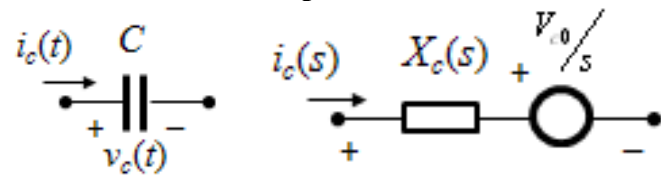
$$V_2 = \frac{R_2}{R_1 + \dots + R_N} v_{IN}$$

## 2 – Time domain

**Models corresponding to the basic elements in “s” domain: Capacitor and Inductor.**

**Capacitor**

**Inductor**



$$i_c(t) = C \frac{dv_c(t)}{dt} ; X_c(s) = \frac{v_c(s)}{i_c(s)} = \frac{1}{Cs}$$

$$v_L(t) = L \frac{di_L(t)}{dt} ; X_L(s) = \frac{v_L(s)}{i_L(s)} = Ls$$

**Normalized transfer function expressions (1st and 2nd. order)**

**1st. order**

**2on. order**

$$H(s) = K \frac{\omega_n}{s + \omega_n} ; \text{ with } \omega_n = \frac{1}{\tau}$$

$$H(s) = K \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}$$

\* Main parameters:

$K$  – Gain Factor (in steady state domain)

$\omega_n$  – Natural angular frequency

$\tau$  – Time constant of the system

\* Main parameters:

$K$  – Gain Factor (in steady state domain)

$\omega_n$  – Natural angular frequency

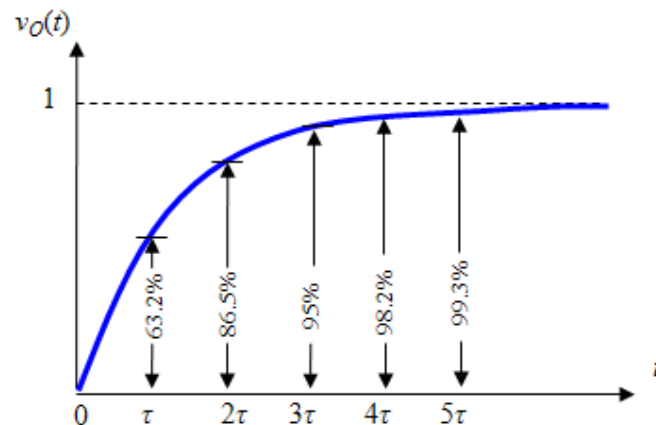
$\xi$  – Damping Factor



## Response to a step unit input

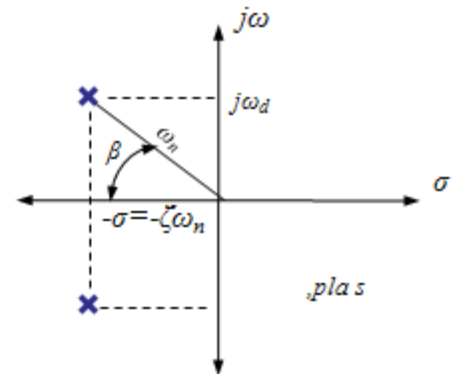
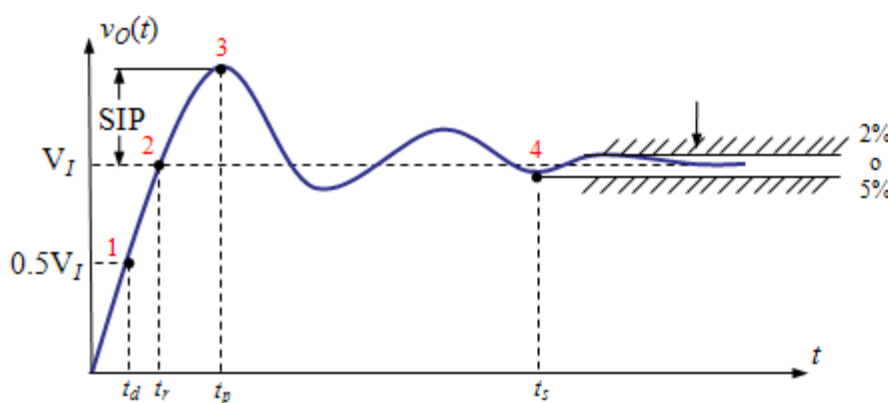
$$H(s) = \frac{v_o(s)}{v_i(s)} \rightarrow v_i(s) = \frac{1}{s}$$

### 1st. order



\*settling time =  $5\tau$

### 2nd. order ( $0 < \xi \leq 1$ )



**Rise time**

**Maximum Overshoot time**

**Overshoot** (expressed in %1)

$$t_r = \frac{1}{\omega_d} \tan^{-1} \left( \frac{\omega_d}{-\sigma} \right) = \frac{\pi - \beta}{\omega_d};$$

$$t_p = \frac{\pi}{\omega_d}$$

$$SIP = \frac{v_o(t_p) - v_o(\infty)}{v_o(\infty)} = e^{-\frac{\xi}{\sqrt{1-\xi^2}}\pi}$$

**Underdamped frequency**

**Settling time**

$$\omega_d = \omega_n \sqrt{1 - \xi^2}$$

$$t_s = \frac{3}{\xi \omega_n} \quad (5\%)$$

### Sinua and Frequency response

The output response to an input sinus  $V_{IP} \sin(\omega t)$  is  $v_o(t) = V_{IP} |H(j\omega)| \sin(\omega t + \angle H(j\omega))$

#### 1er. ordre

#### 2on rdre

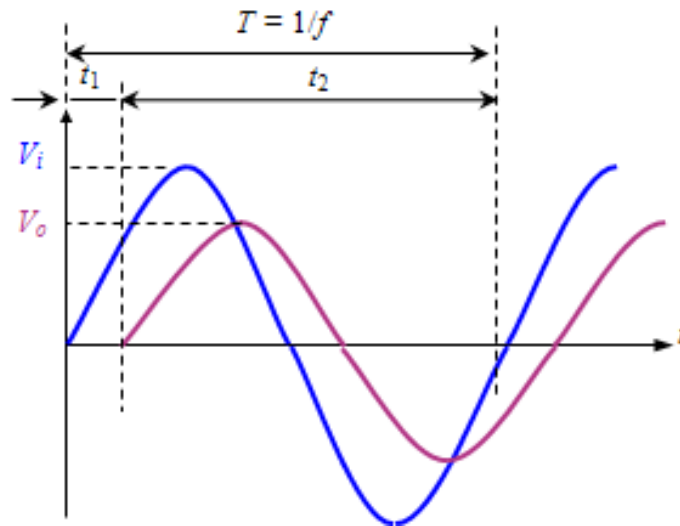
**Módul:**  $|H(j\omega)| = K \frac{\omega_n}{\sqrt{\omega^2 + \omega_n^2}}$

**Modul:**  $|H(j\omega)| = K \frac{\omega_n^2}{\sqrt{(\omega_n^2 - \omega^2)^2 + (2\xi\omega_n\omega)^2}}$

**Fase:**  $\angle H(j\omega) = -\tan^{-1} \left( \frac{\omega}{\omega_n} \right)$

**Fase:**  $\angle H(j\omega) = -\tan^{-1} \left( \frac{2\xi\omega_n\omega}{\omega_n^2 - \omega^2} \right)$

## Module $|H(j\omega)|$ and Phase $\angle H(j\omega)$ estimation from the input and output signals

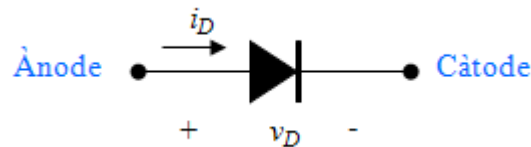


Module:  $H(j\omega) = \frac{V_o}{V_i}$ ; Phase:  $\angle H(j\omega) = \begin{cases} -\frac{t_1}{T} 2\pi, & \text{if } t_1 < t_2 \\ +\frac{t_2}{T} 2\pi & \text{if } t_1 > t_2 \end{cases}$

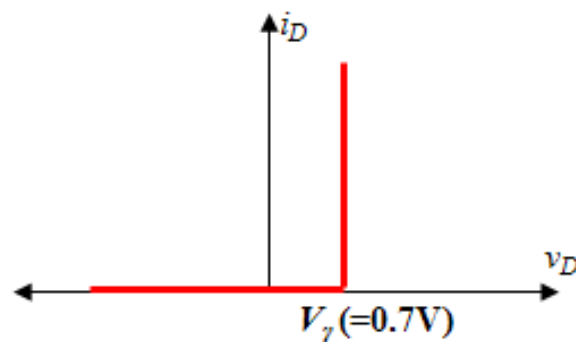
## 2<sup>nd</sup>. Module – Analysis of circuits containing diodes

### Rectifier diode model

Symbol and convention  $i_D - v_D$



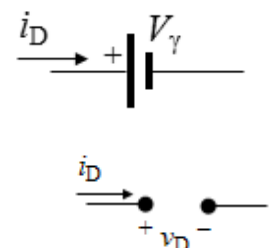
i-v characteristics



\* $V_\gamma$  corresponds to the diode threshold voltage

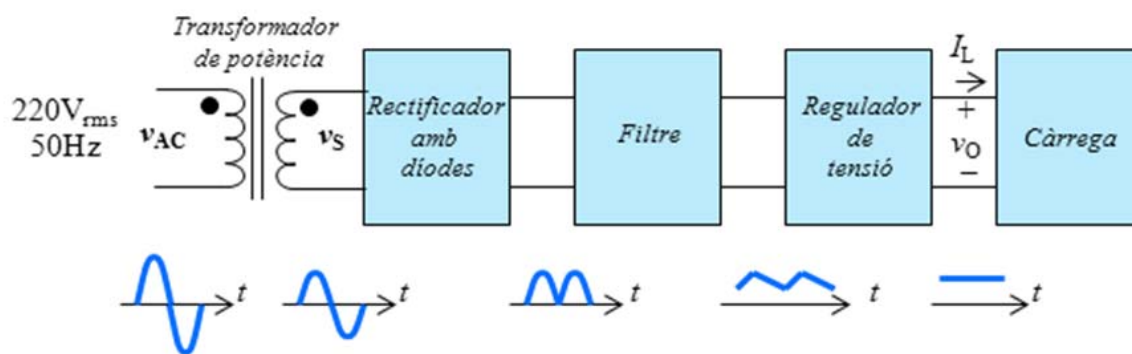
Mathematical model representing its circuit behavior

Operation mode	Condition	Behavior
ON (Conduction mode):	$i_D > 0$	$v_D = V_\gamma$
OFF (Open circuit mode):	$v_D < V_\gamma$	$i_D = 0$



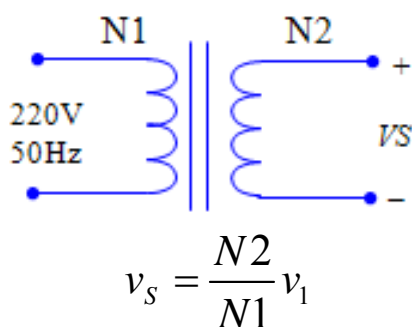
# 1 – DC Power Supply (2on Midterm)

## Block diagram

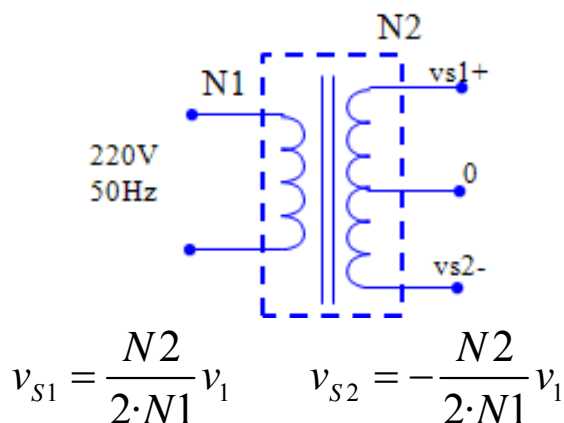


## Transformer

### Single output winding



### Two output windings

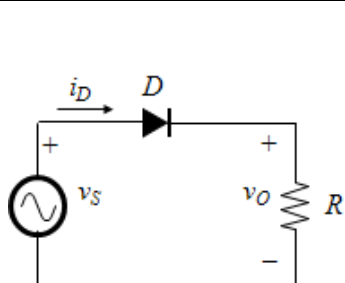


### Conversion from rms to peak value

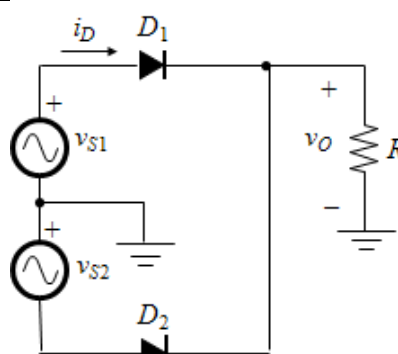
$$v_1 = 220V \text{ rms} \rightarrow V_{1P} = \sqrt{2} v_{s1} \text{ (peak value)}$$

## Rectifiers

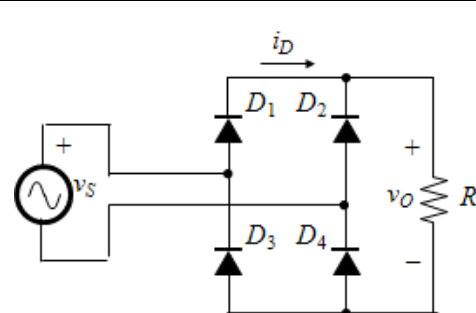
Type



Single-phase half-wave (R1)



Two-phase half-wave (R2)



Single-phase full-wave (R3)

$V_{Omax}$

$$= V_{Smax} - V_\gamma$$

$$= V_{Smax} - 2V_\gamma$$

$V_{O(AV)}$

$$= \frac{V_{Smax}}{\pi} - \frac{V_\gamma}{2}$$

$$= \frac{2V_{Smax}}{\pi} - V_\gamma$$

$$= \frac{2V_{Smax}}{\pi} - 2V_\gamma$$

$V_{RRM}$

$$= V_{Smax}$$

$$= 2V_{Smax}$$

$$= V_{Smax} - V_\gamma$$

$I_{D(AV)}$

$$= \frac{V_{O(av)}}{R}$$

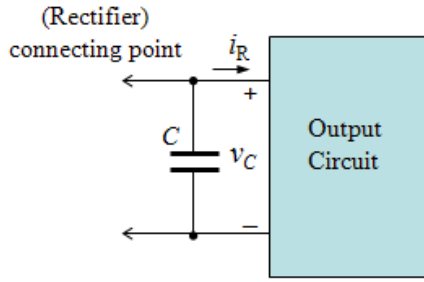
$$= \frac{V_{O(av)}}{2R}$$

$I_{Dmax}$

$$= \frac{V_{Omax}}{R}$$

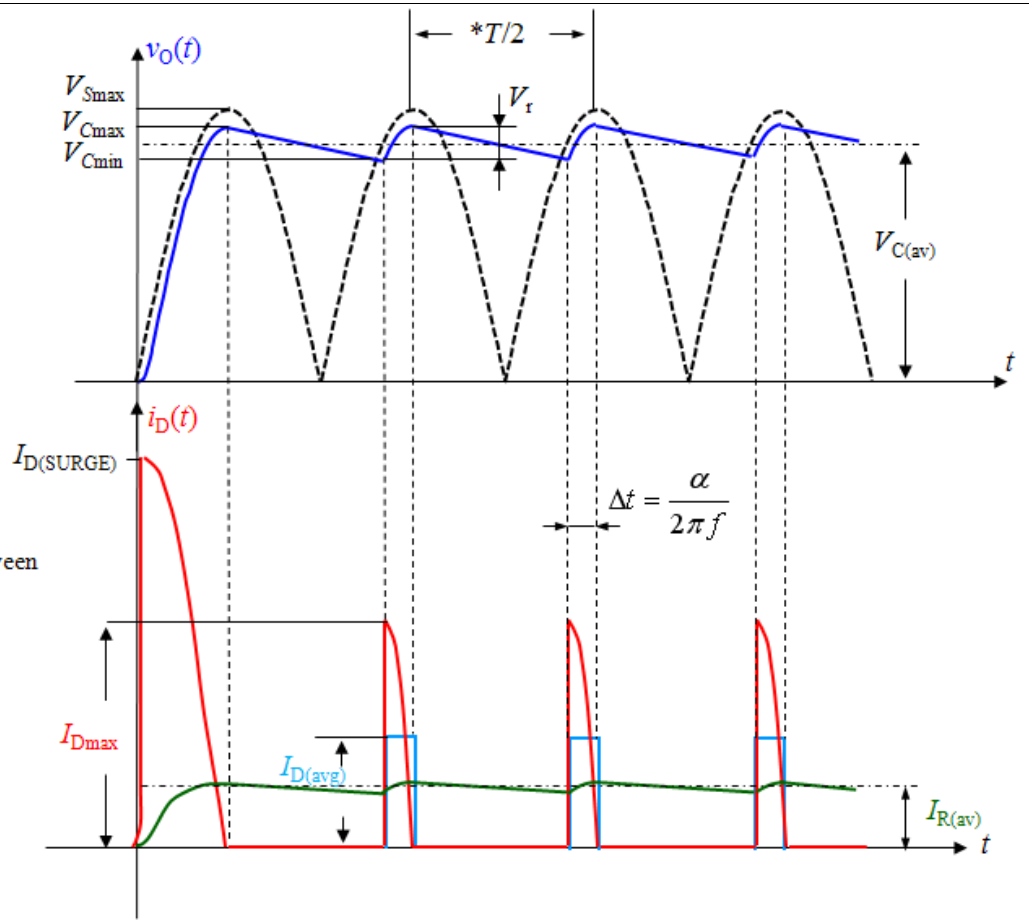
## Filtre de tensió

$$f = \frac{1}{T} = 50 \text{ Hz}$$



Capacitor  $C$  connected in **parallel** between rectifier and output circuit

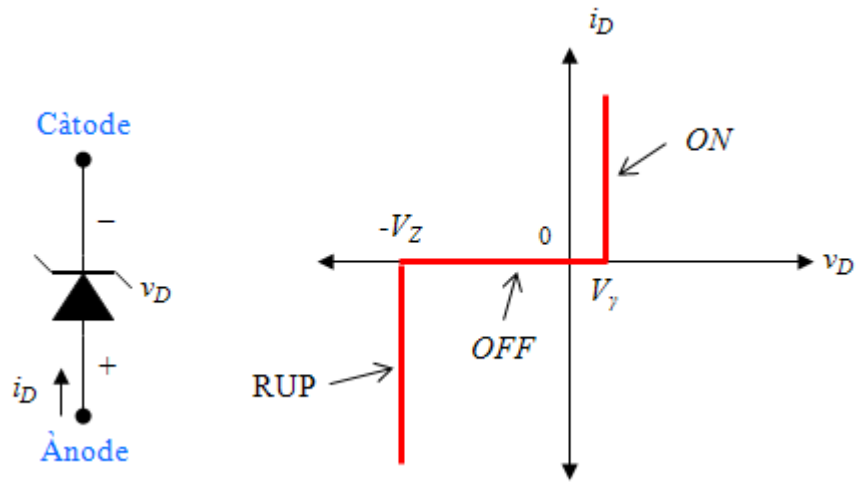
**\*\*** The output circuit can be either a resistor ( $R$ ) or A voltage regulator



\* The discharging time approaches to  $T$  (instead of  $T/2$ ) in the single-phase half-wave rectifier (R1).

Electrical Variable	R1	R2	R3
$V_{Cmax}$	$= V_{Smax} - V_\gamma$		$= V_{Smax} - 2V_\gamma$
$V_r^{**}$ (ripple)	$= \frac{V_{Cmax}}{fRC} \equiv \frac{I_{R(av)}}{fC}$		$= \frac{V_{Cmax}}{2fRC} \equiv \frac{I_{R(av)}}{2fC}$
$\alpha$ (Conduction cycle)	$= 2\pi f \cdot \Delta t = \sqrt{\frac{2V_r}{V_{Cmax}}}$		
$V_{C(av)}$	$V_{Cmax} - \frac{V_r}{2}$		
$V_{RRM}$	$2V_{Cmax} - \frac{V_r}{2}$	$2V_{Cmax} - V_\gamma$	$V_{Cmax} - V_\gamma$
$I_{R(av)}$	$= \frac{V_{C(av)}}{R}$ (only when the output circuit is a resistor of value $R$ )		
$I_{D(SURGE)}$	$= 2\pi f C V_{Smax}$		
$I_{Dmax}$	$= I_{R(av)} \left( 1 + 2\pi \sqrt{2V_{Cmax}/V_r} \right)$	$= I_{R(av)} \left( 1 + 2\pi \sqrt{V_{Cmax}/2V_r} \right)$	
$I_{D(av)}$ (during interval $\Delta t$ )	$= I_{R(av)} \left( 1 + \pi \sqrt{2V_{Cmax}/V_r} \right)$	$= I_{R(av)} \left( 1 + \pi \sqrt{V_{Cmax}/2V_r} \right)$	

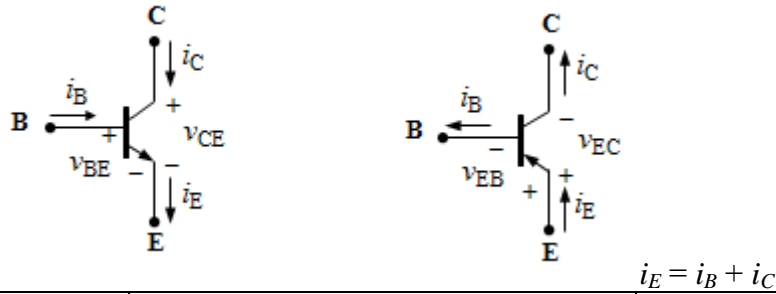
## Zener diode



### Mathematical model

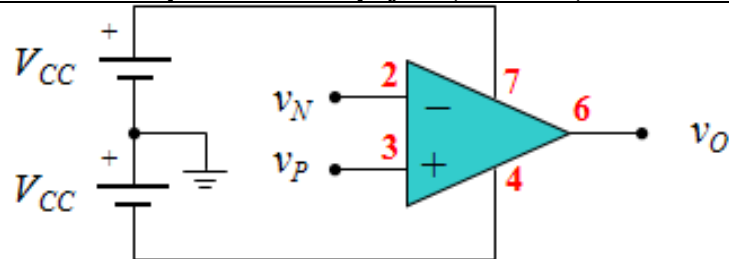
Operating mode	Variable Condition	Variable Behavior
<b>ON (Conduction):</b>	$i_D > 0$	$v_D = V_\gamma$
<b>OFF (Non-conduction):</b>	$-V_Z < v_D < V_\gamma$	$i_D = 0$
<b>RUP (Zener operation):</b>	$i_D < 0$	$v_D = -V_Z$

## Bipolar Junction Transistor – BJT



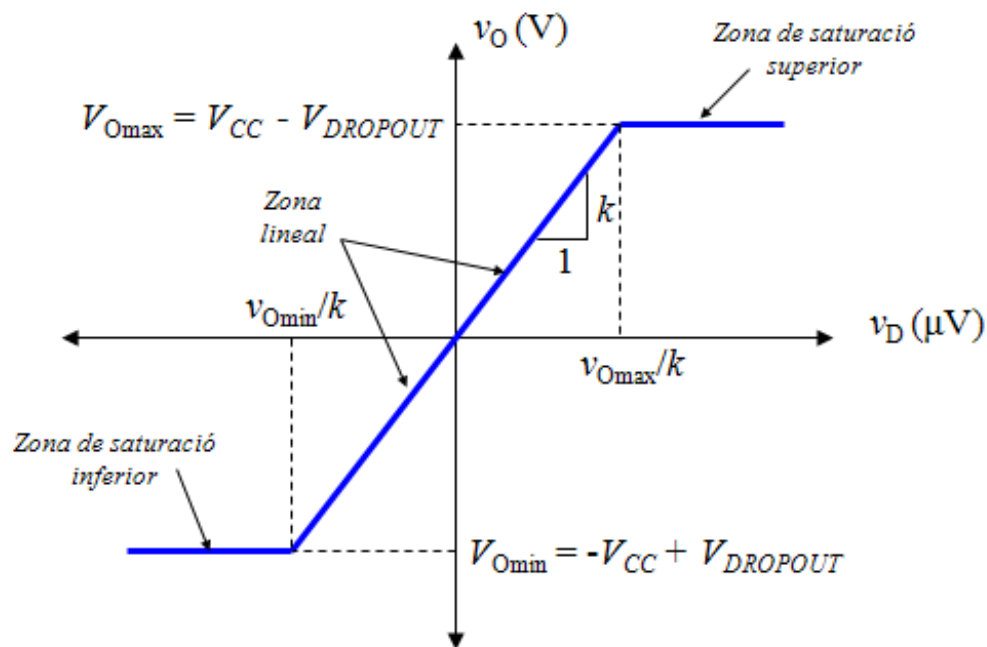
Operating mode	Variable conditions	Variable Behavior
<b>CUT-OFF</b>	$v_{BE} < V_{BE\gamma}, v_{CE} > V_{CE(sat)}$	$i_B = 0, i_C = 0$
<b>ACTIVE</b>	$i_B > 0, v_{CE} > V_{CE(sat)}$	$v_{BE} = V_{BE\gamma}, i_C = \beta i_B$
<b>SATURATION</b>	$i_B > 0, i_C < \beta i_B$	$v_{BE} = V_{BE\gamma}, v_{CE} = V_{CE(sat)}$

## Operational Amplifier (OPAMP)

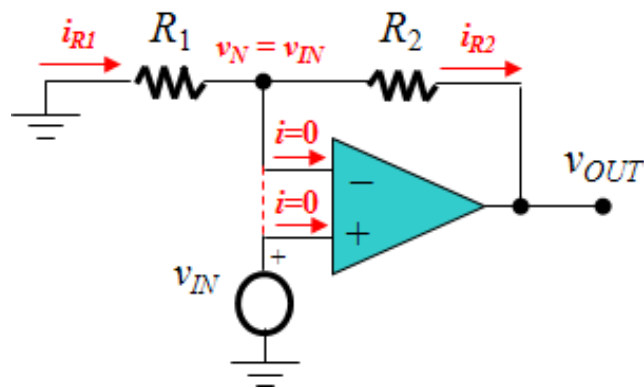


### Mathematical model

$$v_O = \begin{cases} V_{O(max)} & , \text{ if } v_D > \frac{V_{O(max)}}{k} \\ kv_D & , \text{ if } \frac{V_{O(min)}}{k} \leq v_D \leq \frac{V_{O(max)}}{k} \\ V_{O(min)} & , \text{ if } v_D < \frac{V_{O(min)}}{k} \end{cases} ; \quad v_D = v_P - v_N ; \quad k \rightarrow \infty$$



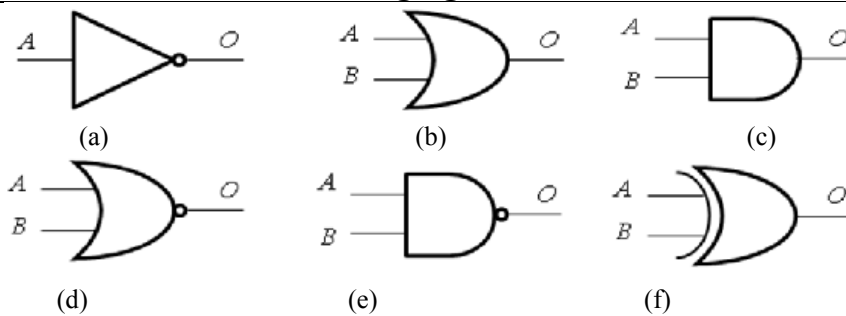
- “Virtual shortcircuit” when approximating to ideal behavior



Virtual shortcircuit concept:  $i_N = i_P = 0$  ( $i_{R1} = i_{R2}$ )  $v_N = v_P = v_{IN}$  ( $v_D = 0$ )

### 3 – Digital Systems

#### Logic gates



Comb.	A	B	NOT	OR	AND	NOR	NAND	OR-E
1	0	0	1	0	0	1	1	0
2	0	1	1	1	0	0	1	1
3	1	0	0	1	0	0	1	1
4	1	1	0	1	1	0	0	0
Funció			$Y = \bar{A}$	$Y = A + B$	$Y = AB$	$Y = \overline{A + B}$	$Y = \overline{AB}$	$Y = A \oplus B$

#### Morgan Laws

$$\overline{A + B} = \bar{A} \bar{B}$$

$$\overline{AB} = \bar{A} + \bar{B}$$